



**B.Tech III Semester Supplementary Examinations, July 2024**

**SWITCHING THEORY AND LOGIC DESIGN**

(Common to EEE & ECE)

**Maximum Marks: 70**

**Date: 18.07.2024 Duration: 3 hours**

- Note:
1. This question paper contains two parts A and B.
  2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
  3. Part B consists of 5 Units. Answer any one full question from each unit which carries 10M.
  4. Each question carries 10 marks and may have a, b, c, d as sub questions.

**Part-A**

All the following questions carry equal marks		(10X2M=20 Marks)	CO	Bloom Tx
1	What is Gray code?		1	L1
2	What is min term?		1	L1
3	What are don't cares?		2	L1
4	Write about 2X1 MUX.		2	L1
5	Compare latch and flip flop.		3	L1
6	Write the characteristic table of SR Flip flop.		3	L1
7	Compare combinational and sequential circuits.		4	L1
8	Explain about Ring counter with a neat diagram.		4	L1
9	List the capabilities of finite state machine.		5	L1
10	Compare Mealy and Moore machines.		5	L1

**Part-B**

Answer All the following questions.		(5X10M=50Marks)		
11	a) Convert the given Gray code number to equivalent binary. [5M] 001001011110010. b) Convert (A0F9.0DC) <sub>16</sub> to decimal, binary, octal. [5M]		1	L2
<b>OR</b>				
12	Simplify the following Boolean expressions using the Boolean theorems. [10M] (i) $(A+B+C)(B'+C) + (A+D)(A'+C)$ (ii) $(A+B)(A+B')(A'+B)$		1	L2
13	Minimize the following expressions using K-map and realize using NAND Gates. $f = \sum m(1, 3, 5, 8, 9, 11, 15) + d(2, 13)$ . [10M]		2	L2
<b>OR</b>				
14	Reduce the expression using k map $F(A, B, C, D, E) = \sum(0, 1, 3, 4, 5, 7, 10, 11, 12)$ and implement the real minimal expression in universal logic. [10M]		2	L2

15	Realize 16:1 MUX using 8:1 MUX. [10M]	3	L2
	OR		
16	What is meant by Edge triggered? Differentiate SR-FF and JK-FF with their functional operation and excitation tables. [10M]	3	L2
17	a). Draw the logic diagram of a SR latch using NOR gates. Explain its operation using excitation table. [5M] b) Convert D flip-flop into T and JK flip-flops. [5M]	4	L2
	OR		
18	Design and explain a synchronous MOD-12 down-counter using T flip-flop. [10M]	4	L2
19	a) What are the Moore and Mealy machines? Compare them. [5M] b) Explain the procedure for state minimization using the partition technique. [5M]	5	L2
	OR		
20	Draw the diagram of Mealy type FSM and explain with an example. [10M]	5	L2