R20 Regulation *Subject code: 3P4EB*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech IV Semester Supplementary Examinations, February 2024

Computer Organization and Architecture

(Computer Science & Engineering)

Maximum Marks: 70 Date:19.02.2024 Duration: 3 hours

Note: 1.This question paper contains two parts A and B.
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit which carries 10M.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

	Part-A		
All the following questions carry equal marks (10x2M=20 Marks)		CO	Bloom Tx
1	Define Computer architecture and computer organization.	CO1	L1
2	What is the function of following registers: MAR, IR, PC, Y?	CO1	L1
3	What are the advantages and disadvantages of Hardwired Control Unit?	CO2	L1
4	How 16-bit address is converted into 20-bit address in 8086?	CO2	L1
5	What are the main features of Booth's algorithm?	CO3	L1
6	Define the algorithm for restoring division.	CO3	L1
7	List out the methodologies involved in handling Priority Interrupt.	CO4	L1
8	What is auxiliary memory in computer architecture?	CO4	L1
9	What is an Instruction pipeline?	CO5	L1
10	What is synchronization?	CO5	L1
	Part-B		
Answer All the following questions. (5X10M=50Marks)			
11	A. Explain the basic operational concept involved in the execution of an instruction with an example. (5M) B. Explain the function of each functional unit in the computer system. (5M)	CO1	L2 L2
	OR		
12	What are the different phases a basic computer instruction cycle consists? Explain the instruction cycle with flowchart. (10M)	CO1	L2
13	Explain the operation of a Micro programmed control unit using a diagram. (10M)	CO2	L2
	OR		
14	With the help of neat block diagram, explain the internal architecture of 8086 microprocessor. (10M)	CO2	L5
15	Explain the algoritham of Addition and Subtraction with signed magnitude data in computer architecture. (10M)	CO3	L2

	OR		
16	A. Explain about typical Data Transfer Instructions. (5M) B. Write the multiplication algorithm and explain with an example. (5M)	CO3	L2 L2
17	Explain Daisy-Chaining priority and Parallel priority Interrupt with its hardware diagram. (10M)	CO4	L2
	OR		
18	A. What is virtual memory? Explain the relation between address space and memory space in a virtual memory system along with its memory table for mapping. (5M) B. Explain about Cache memory. (5M)	CO4	L1 L2
19	A. Write about pipelining and its importance in high-speed applications. (3M) B. Demonstrate the pipeline organization for following example $A_i*B_i+C_i$ for i =1,2,3,... (7M)	CO5	L2 L2
	OR		
20	A. Explain the Characteristics of multi-processor. (5M) B. Compare tightly coupled and loosely coupled multiprocessors. (5M)	CO5	L2 L3