R20 Regulation *Subject code: 3P4BB*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech IV Semester Supplementary Examinations, February 2024

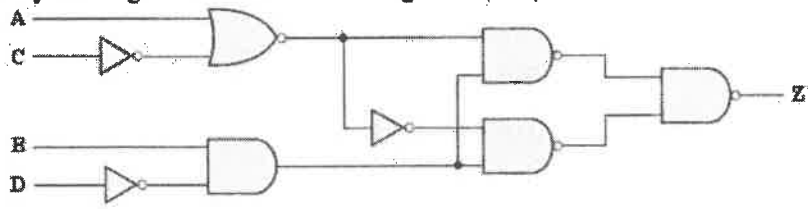
DIGITAL ELECTRONICS

(Electrical & Electronics Engineering)

Maximum Marks: 70 Date:19.02.2024 Duration: 3 hours

Note: 1.This question paper contains two parts A and B.
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit which carries 10M.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

	Part-A		
All the following questions carry equal marks (10x2M=20 Marks)		CO	Bloom Tx
1	Convert 2598.67510 (Decimal) to Hexadecimal.	CO1	L1
2	Given the two binary numbers X = 1010101 and Y = 1001011, perform the subtraction X-Y using 1's complements.	CO1	L1
3	Which gates are called as the universal gates? What are its advantages?	CO2	L1
4	State the limitations of Karnaugh map.	CO2	L1
5	What is combinational circuit? Give examples.	CO3	L1
6	Express Gray code 10111 into Binary number.	CO3	L1
7	What is the difference between latch and flip flop?	CO4	L1
8	Mention any two differences between the edge triggering and level triggering.	CO4	L2
9	What are the capabilities and limitations of Finite state machines?	CO5	L1
10	Define the the Moore and Mealy machines.	CO5	L1
	Part-B		
Answer All the following questions. (5X10M=50Marks)			
11	A. Convert $(105.589)_{10}$ decimal number to octal number. (2M) B. Convert $(1693.0628)_{10}$ decimal fraction to hexadecimal fraction $(\ )_{16}$ (2M) C. Convert $(128)_8 = (\ )_{10}$ (2M) D. Convert $(EF.B1)_{16} = (\ )_{10}$ (2M) E. Convert $(1A.2B)_{16}$ to $(\ )_8$ (2M)	CO1	L2
	OR		
12	Generate 7-bits Hamming code for below message bits. (10M) (A)1011 (B) 0111	CO1	L3
13	Using K-map method, Simplify the following Boolean function and obtain (a) minimal SOP and (b) minimal POS expression and realize using only NAND and NOR gates $F=\sum_m (0,2,3,6,7) + d(8,10,11,15)$ (10M)	CO2	L4

	OR		
14	A. Simplify the following function using K – map, f=ABCD+AB'C'D'+AB'C+AB and realize the SOP using only NAND gates and POS using only NOR gates. (7M) B. Simplify the logic circuit shown in figure. (3M) 	CO2	L4
15	A. Implement the following function using suitable multiplexer F (A, B, C, D) = Σ(1, 3, 4, 11, 12, 13, 14, 15) (5M) B. Draw the logic diagram of a 2-bit by 2-bit binary multiplier and explain its operation. (10M)	CO3	L4
	OR		
16	Draw the block schematic of Magnitude comparator and explain its operation. (10M)	CO3	L3
17	A. Draw and explain the logic diagram for a 5- bit serial load shift register using D FF. (5M) B. Explain the working Master/Slave JK FF. (5M)	CO4	L3
	OR		
18	A. Design a synchronous 3-bit counter which counts in the sequence 1, 3, 2, 6, 7, 5, 4, (repeat) 1,3..... using T FF. (5M) B. Design and working of a synchronous MOD- 5 counter. (5M)	CO4	L3
19	Explain the procedure of state minimization using the partition technique. (10M)	CO5	L3
	OR		
20	A. Discuss the Finite state machine capabilities and limitations in briefly. (3M) B. Explain about the Merger Graphs and Merger Tables. (7M)	CO5	L3