R20 Regulation *Subject code: 3P3DB*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech III Semester Supplementary Examinations, February 2024

DIGITAL LOGIC DESIGN

(ECE)

Maximum Marks: 70 Date: 21.02.2024 Duration: 3 hours

Note:
1. **This question paper contains two parts A and B.**
2. **Part A is compulsory which carries 20 marks. Answer all questions in Part A.**
3. **Part B consists of 5 Units. Answer any one full question from each unit.**
4. **Each question carries 10 marks and may have a, b, c, d as sub questions.**

Part-A

All the following questions carry equal marks (10X2M=20 Marks)		CO	Bloom Tx
1	Find the 2's complement and 1's complement of binary number (101101)	CO1	L1
2	Convert the binary number (1101100010011011) into hexadecimal number.	CO1	L2
3	What are the universal gates ? Why they called as universal gates?	CO2	L1
4	What are the De Morgan's theorems?	CO2	L1
5	Draw the basic circuit of half adder and mention the truth table	CO3	L1
6	Define a 2x1 MUX.	CO3	L1
7	What is the difference between Latch and Flip flop?.	CO4	L2
8	What is the characteristic equation of D and T flip flop?	CO4	L1
9	Define finite state machine	CO5	L1
10	List the limitations of finite state machines	CO5	L1

Part-B

Answer All the following questions. (5X10M=50Marks)				
11	(a) Convert the hexadecimal number 68BE to binary and then from binary convert it to octal (b) Convert the following to Decimal then to Octal a) (125F)16 b) (10111111)2	5M 5M	CO1	L2 L2
	OR			
12	(a) What is a Binary Coded Decimal? Explain its Properties. (b) Explain how to convert from binary to hexadecimal number with an example. Mention the advantages of hexadecimal system.	5M 5M	CO1	L2 L2
13	(a) Implement AND,OR and NOR by using NAND gate. (b) Simplify the following Boolean function using three variable maps. F(x,y,z) =∑(0,2,6,7)	5M 5M	CO2	L4 L4
	OR			
14	(a) Show that the dual of the exclusive OR is also its compliment. (b) Demonstrate by means of truth tables the Boolean Associate law and Distributive law	5M 5M	CO2	L1 L2

15	(a)Design a Full adder using two half adders (b)Construct a 16x1 multiplexer with two 8x1 and one 2x1 multiplexer	5M 5M	CO3	L4 L3
	OR			
16	(a)Explain about Decoder and implement the 4x16 Decoder. (b)What is a Priority encoder? Explain with an example.	5M 5M	CO3	L2 L2
17	(a) Draw the block diagram of asynchronous sequential circuit. Explain. (b)Explain the operation of 4 bit binary counter	5M 5M	CO4	L2 L2
	OR			
18	(a)What is a sequential circuit? Explain the Latch using NOR gate. (b)Using D flip flops and wave forms explain the working of a 4bit SISO shift register	5M 5M	CO4	L2 L2
19	(a)With a neat block diagram , explain the Moore model of clocked sequential circuit. (b)Discuss about state diagrams with necessary diagrams.	5M 5M	CO5	L4 L2
	OR			
20	(a) What are the capabilities of Finite State Machine ? discuss (b)Write the differences between Mealy and Moore machines.	5M 5M	CO5	L4 L2