R18 Regulation *Subject code: 2P3DB*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech III Semester Supplementary Examinations, February 2024

DIGITAL LOGIC DESIGN

(ECE)

Maximum Marks: 70 Date:19.02.2024 Duration: 3 hours

Note: **1.This question paper contains two parts A and B.**
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit which carries 10M.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

	All the following questions carry equal marks (10X2M=20 Marks)	**CO**	**BTL**
1	What is Gray code?	CO1	L1
2	What are the universal gates and why those are called as universal gates?	CO1	L1
3	Define minterm and maxterm	CO2	L1
4	Design 2 × 1 Multiplexer with neat logic diagram.	CO2	L2
5	Write characteristic table of SR Flip flop with logic diagram.	CO3	L1
6	Explain about binary cell.	CO3	L2
7	What is meant by mod-10 Counter?	CO4	L1
8	Differentiate RAM and ROM memories.	CO4	L2
9	What is state diagram?	CO5	L1
10	Define Mealy and Moore sequential state machines.	CO5	L1

Part-B

	Answer All the following questions. **(5X10M=50Marks)**		**CO**	**BTL**
11	a) Write the decimal numbers 9,6 and 3 in terms of the following weighted binary codes: i) 4,2,2,1 ii) 2,4,2,1 iii) 8,4,2,1 iv) Gray Code v) Excess-3 Code b) Prove that AB'C + B + BD'+ ABD'+ A'C = B + C.	5M 5M	CO1	L4 L4
	OR			
12	Design a circuit to convert Excess-3 code to BCD code using discrete Logic gates	10M	CO1	L4
13	Simplify the expression F(A,B,C,D)=A$\bar{B}$+AB$\bar{D}$+ABD+$\bar{A}\bar{C}\bar{D}$+$\bar{A}$B$\bar{C}$ and implement with NAND gates only.	10M	CO2	L4
	OR			
14	a)Draw the truth table for full adder and design it using two Half Adders. b) Implement full adder with Decoder and also with Multiplexers.	5M 5M	CO2	L3 L3
15	Define Multiplexer and explain the procedure to implement 32X1 MUX by Using 4X1 multiplexers	10M	CO3	L3

	OR			
16	Design 2-bit digital comparator and explain with neat sketch.	10M	CO3	L3
17	a) Convert D flip-flop into T flip-flop. b) Convert D flip-flop into JK flip-flop.	5M 5M	CO4	L3 L3
	OR			
18	What do you mean by universal shift register? Draw and explain its circuit diagram and operation.	10M	CO4	L3
19	Explain about sequential circuits, state table and state diagram	10M	CO5	L3
	OR			
20	Explain about Mealy machine with circuit diagram	10M	CO5	L3