Regulation R17 *Subject code:1P4DA*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech II Year II Semester Supplementary Examinations, February 2024

Switching Theory and Logic Design

(Electronics and Communication Engineering)

Maximum Marks: 70 Date:16.02.2024 **Duration: 3 Hours**

Note: **1.This question paper contains two parts A and B.**
2. Part A is compulsory which carries 10 marks. Answer all questions in Part A.
3. Part B consists of 10 questions. Answer any 5 questions which carries 12M.
4. Each question carries 12marks and may have a, b, c, d as sub questions.

	Part-A	
All the following questions carry equal marks		(10X2M=20 Marks)
1	What is Gray code?	
2	How do you obtain dual of an expression?	
3	What are don't cares?	
4	What is minterm?	
5	Compare combinational and sequential circuits.	
6	Explain about binary cell.	
7	What are the basic types of shift registers?	
8	Compare asynchronous and synchronous counters.	
9	Explain capabilities of finite state machine.	
10	Explain concept of minimal cover table.	
	Part-B	
Answer all the questions		(10MX 5=50Marks)
11	a) Convert the gray number 101101 into decimal, hex, octal b) Perform the subtraction in BCD using 9's complement method for 592.6-887.9	[5+5]
	OR	
12	Derive the Boolean expression for a two input Ex-OR gate to realize with the two input NAND gates without using complemented variables and draw the circuit.	[10]
13	Expand (A+D')(A+C')(A'+B)(A'+B+C) into max terms and min terms.	[10]
	OR	
14	Minimize the following expression using K-map and realize using NAND Gates. F (A,B,C,D) = ∑m (0,1,2,9,11) +d(8,10,14,15).	[10]
15	Explain about Multiplexer .Design a 32X1 multiplexer using 4x1 multiplexer.	[10]
	OR	
16	Draw the circuit diagram of J-K flip flop with NAND gates and explain its operation with the help of truth table. How race around condition is eliminated.	[10]
17	a) Explain about serial in parallel out shift register with a neat diagram. b) Design a synchronous counter with T-flip flops that goes through the binary repeated sequence 0,1,3,7,6,4,0,1…..	[5+5]

	OR	
18	Design a mod-12 Ripple counter using T flip flops and explain its operation.	[10]
19	Explain about sequential circuits, state table and state diagram.	[10]
	OR	
20	Explain about Mealy machine with circuit diagram.	[10]