R20 Regulation *Subject code:3P6DD*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech VI Semester Regular/Supplementary Examinations, July 2024

VLSI DESIGN

(ECE)

Maximum Marks: 70 Date:26.07.2024 Duration: 3 hours

Note: **1.This question paper contains two parts A and B.**
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit which carries 10M.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

	Part-A		
All the following questions carry equal marks (10X2M=20 Marks)		CO	Bloom Tx
1	Define g_m of MOS transistor.	CO1	L1
2	Why NMOS technology is preferred more than PMOS technology?	CO1	L4
3	Write a short note on scaling.	CO2	L2
4	Explain difference between stick diagram and layout diagram.	CO2	L4
5	What is switch logic?	CO3	L1
6	Explain the importance of wiring capacitance of a MOS transistor.	CO3	L2
7	Design a 2-bit Parity generator.	CO4	L5
8	Describe the 1T DRAM.	CO4	L2
9	Explain about test Principles used for testing.	CO5	L2
10	Differentiate PLA and PAL.	CO5	L4
	Part-B		
Answer All the following questions. (5X10M=50Marks)			
11	Explain with neat diagrams the various NMOS fabrication technology. [10]	CO1	L2
	OR		
12	Derive the value of Zpu/Zpd of inverter driven by another inverter. [10]	CO1	L2
13	Explain the various steps involved in VLSI design flow in detail. [10]	CO2	L2
	OR		
14	Design a Stick Diagram and Layout for 2-input NAND gate. [10]	CO2	L3
15	What are the alternate gate circuits are available? Explain any two of item with suitable sketch. [10]	CO3	L2
	OR		
16	A. Draw and explain fan-in and fan-out characteristics of different CMOS design technologies. [5] B. Illustrate the significance of Choice of Layers. [5]	CO3	L3&L2
17	Explain 6-T SRAM operation with neat sketch. [10]	CO4	L2
	OR		
18	A. Design and implement 4-bit ripple carry adder. [5]	CO4	L5&L2

	B. Explain Barrel shifter with a neat diagram. [5]		
19	A. What is CPLD? Draw its basic structure and give its applications. [5] B. Compare CPLDs and FPGAs. [5]	CO5	L2&L3
	OR		
20	Explain chip level test techniques with techniques. [10]	CO5	L2