



R20 Regulation

Subject code:3P6BD

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech VI Semester Regular/Supplementary Examinations, July 2024

MICROPROCESSORS AND MICROCONTROLLERS

(EEE)

Maximum Marks: 70

Date:26.07.2024 Duration: 3 hours

- Note:
- 1.This question paper contains two parts A and B.
 2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
 3. Part B consists of 5 Units. Answer any one full question from each unit which carries 10M.
 4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks (10X2M=20 Marks)		CO	Bloom Tx
1	List out different segmentations presented in 8086 Microprocessor.	CO1	I
2	What is the maximum memory size that can be addressed by 8086?	CO1	I
3	Give the importance of memory interfacing of 8051.	CO2	I
4	Name the five interrupt sources of 8051.	CO2	I
5	Give the serial communication standards.	CO3	I
6	What is the function of ADC and DAC?	CO3	I
7	Mention the advantages of ARM processor.	CO4	II
8	Name the special purpose registers in ARM processor.	CO4	I
9	List the applications of the OMAP processor.	CO5	I
10	Give the difference between OMAP and CORTEX processors.	CO5	II

Part-B

Answer All the following questions. (5X10M=50Marks)			
11	Express the categories under which the instructions in the instruction set of 8086 microprocessors are grouped. Explain the operation of instructions in any two groups. [10]	CO1	II
OR			
12	Draw the pin diagram of 8086 processor and explain all the signals. [10]	CO1	II
13	With a functional block diagram, discuss the architecture of 8051 microcontroller. [10]	CO2	II
OR			
14	Discuss the different types of addressing modes supported by 8051 microcontrollers with examples. [10]	CO2	II
15	Explain the interfacing of keyboard using 8051 microcontrollers with diagram. [10]	CO3	II
OR			
16	Describe operation of SPI bus. [10]	CO3	II

17	Discuss registers of ARM Processor in details. [10]	CO4	II
	OR		
18	Describe the Interrupts, vector table and exception handler in ARM. [10]	CO4	II
19	Draw and explain the register organization of CORTEX processor. [10]	CO5	II
	OR		
20	Give an account of OMAP architecture with a block diagram. [10]	CO5	II