R20 Regulation *Subject code: 3E5DA*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech V Semester Supplementary Examinations, July 2024

DIGITAL DESIGN THROUGH VERILOG HDL

(ECE)

Maximum Marks: 70 Date:01.08.2024 Duration: 3 hours

Note: **1.This question paper contains two parts A and B.**
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

	Part-A	CO	Bloom Tx
All the following questions carry equal marks (10X2M=20 Marks)			
1	List the applications of Verilog HDL.	CO1	L2
2	Define Keywords and Identifiers.	CO1	L1
3	What is array of Instances of primitives?	CO2	L1
4	Why delay is used in Verilog?	CO2	L2
5	Give the difference between bitwise operator and logical operator.	CO3	L2
6	Draw the circuit diagram of CMOS inverter.	CO3	L2
7	Mention the types of conditional statements?	CO4	L1
8	What is sequential circuit testing?	CO4	L1
9	Why can't we use task inside function method in Verilog?	CO5	L2
10	How the sequential UDPs differ from combinational UDP?	CO5	L2
	Part-B		
Answer All the following questions. (5X10M=50Marks)		CO	
11	Explain the steps of specification and logic design in ASIC design flow. (10M)	CO1	L2
	OR		
12	A. What do you understand by comments used in Verilog? Also explain different comments used in Verilog. B. How many types of number specification in Verilog? Explain it. (5M+5M)	CO1	L2
13	Write Verilog Code for 4:1 MUX using Gate Level Modelling. (10M)	CO2	L3
	OR		
14	Write a Verilog code for 4-bit ripple carry full adder using the gate-level model. (10M)	CO2	L3
15	A. Write a Verilog HDL code for n-bit right-to-left shift register using data flow level. B. Explain about operator priority with examples. (5M+5M)	CO3	L3
	OR		
16	Design a CMOS Nand gate using NMOS and PMOS transistors with verlog code and test bench. (10M)	CO3	L6

17	A. What are the differences between an initial behavior and an always behavior? B. Design a Multifunction JK Flip-flop using behavioral modelling. (5M+5M)	CO4	L4
	OR		
18	A. Explain the Procedural Assignments with example. B. Design a BCD to 7-Segment Decoder using behavioral modelling. (5M+5M)	CO4	L6
19	A. Design Verilog module using path delay. B. Explain parameters in Verilog. (5M+5M)	CO5	L6
	OR		
20	Describe how to use combinational and sequential UDPs. (10M)	CO5	L4