R18 Regulation *Subject code: 2P6DB*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech VI Semester Supplementary Examinations, July 2024

MICROPROCESSORS AND MICROCONTROLLERS
(ECE)

Maximum Marks: 70 Date:22.07.2024 Duration: 3 hours

Note: 1.This question paper contains two parts A and B.
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit which carries 10M.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

	Part-A		
All the following questions carry equal marks (10X2M=20 Marks)		CO	Bloom Tx
1	Write Register addressing mode of 8086 microprocessor with two examples.	1	L1
2	Discuss the features of 8086 microprocessor.	1	L1
3	Categorize Register Banks of RAM in 8051.	2	L1
4	Draw TMOD register.	2	L1
5	Explain the PSEN & EA signals in 8051.	3	L1
6	Write short notes on RAM and ROM.	3	L1
7	List any 3 features of ARM.	4	L1
8	List 3 differences between ARM instruction set and Thumb instruction set.	4	L1
9	Mention applications of CORTEX processor.	5	L1
10	Explain different applications of OMAP-Processor.	5	L1
	Part-B		
Answer All the following questions. (5X10M=50Marks)			
11	Explain the Architecture of 8086 Microprocessor with a neat sketch. [10]	1	L2
	OR		
12	List and Explain 8086 Microprocessor Data Transfer instructions with examples. [10]	1	L2
13	With a neat diagram, describe the internal architecture of 8051 Microcontroller. [10]	2	L2
	OR		
14	Explain the following SFR's of 8051 microcontroller in detail. a)TMOD b) TCON. [10]	2	L2
15	Write short notes on Serial Communication standards and Explain SPI BUS. [10]	3	L2
	OR		
16	Explain Interfacing of D to A Converter with 8051 Microcontroller. [10]	3	L2

17	Draw ARM Programming Model and explain it. [10]	4	L2
	OR		
18	Explain Data Processing Instructions of ARM Processor. [10]	4	L2
19	With a neat diagram, explain the Architecture of CORTEX Processor. [10]	5	L2
	OR		
20	Draw and explain the functional diagram of OMAP Processor. [10]	5	L2