R18 Regulation *Subject code: 2P5DB*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech V Semester Supplementary Examinations, July 2024

VLSI DESIGN
(ECE)

Maximum Marks: 70 Date:22.07.2024 Duration: 3 hours

Note: 1.This question paper contains two parts A and B.
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit which carries 10M.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

	Part-A		
All the following questions carry equal marks (10X2M=20 Marks)		CO	Bloom Tx
1	What is body effect?	1	L1
2	Define figure of merit.	1	L1
3	Define scaling.	2	L1
4	What is stick diagram?	2	L1
5	Define Risetime.	3	L1
6	Define fan out.	3	L1
7	Draw the circuit diagram of DRAM cell.	4	L2
8	What is comparator?	4	L1
9	Implement Half adder using PAL.	5	L2
10	Define observability with respect to testing.	5	L1
	Part-B		
Answer All the following questions. (5X10M=50Marks)			
11	With neat sketches explain BICMOS fabrication in an n-well process. [10M]	1	L3
	OR		
12	Explain the operation of NMOS enhancement transistor. [10M]	1	L2
13	Draw the flow chart of VLSI Design flow and explain the operation of each step-in detail [10M]	2	L2
	OR		
14	Draw the CMOS logic circuit, stick diagram and layout for the following Boolean expression F = [A.(B+C)]'. [10M]	2	L3
15	Explain in detail about Dynamic CMOS logic and CMOS Domino logic gates with suitable example. [10M]	3	L2
	OR		
16	Describe three sources of wiring capacitance. [10M]	3	L3

17	a) Draw the logic diagram of zero/one detector and explain its operation. [5M] b) Explain about ALU subsystem. [5M]	4	L2
	OR		
18	a) Design a four-bit parity generator using only XOR gates. [5M] b) Draw the circuit diagram of carry select adder and explain it. [5M]	4	L3 L3
19	Explain the architecture of FPGA with neat diagram. [10M]	5	L2
	OR		
20	Discuss chip level testing techniques. [10M]	5	L3