



RI7 Regulation

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

Subject code:1P5DB

B.Tech III Year I Semester Supplementary Examinations, July 2024

LINEAR & DIGITAL IC APPLICATIONS

(ECE)

Maximum Marks: 70

Date:22.07.2024 Duration: 3 hours

- Note:
1. This question paper contains two parts A and B.
 2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
 3. Part B consists of 5 Units. Answer any one full question from each unit.
 4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks

(10X2M=20 Marks)

- 1 What is slew rate?
- 2 List features of 741 op-amp.
- 3 Write the relation between lock range and capture range in a PLL.
- 4 Draw the frequency response characteristics of a notch filter.
- 5 Define Quantization error.
- 6 Mention the advantages of R-2R ladder DAC.
- 7 Define noise margin and propagation delay.
- 8 Discuss about parity generator/checker IC.
- 9 What is race around condition? How is it avoided?
- 10 List the basic types of shift registers interns of data movement.

Part-B

Answer All the following questions.

(10M X 5=50Marks)

11. Explain various DC and AC characteristics of an op-amp. (10)
OR
12. Explain the operation of Integrator and plot its output waveforms for different inputs. (10)
13. Explain triangular waveform generator using IC 741 and derive frequency of oscillations.(10)
OR
14. Draw the block diagram of 565 PLL and explain about each block. (10)
- 15.a With neat diagram explain working of weighted resistor DAC. (5)
b Compare weighted resistor DAC and R-2R ladder DAC. (5)
OR
- 16.a Explain the working of a parallel comparator type A/D converter. (5)
b Write the specifications of ADC. (5)
- 17.a Design BCD to gray code converter. (5)

b Design 16-bit comparator using 74LS185 IC. (5)

OR

18 Explain with neat diagram interfacing of TTL gate driving CMOS and CMOS driving TTL Gates. (10)

19 Differentiate between ripple counter and synchronous counter? Design a 3- bit synchronous counter. (10)

OR

20.a Draw and explain 4-bit universal shift register. (5)

b Design a Modulo-12 ripple counter using 74×74. (5)