



R17 Regulation

Subject code: 1E6DD

# TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

**B.Tech. III Year II Semester Supplementary Examinations, July 2024**

## VLSI Design

(ECE)

Maximum Marks: 70

Date:30.07.2024 Duration: 3 hours

- Note:
1. This question paper contains two parts A and B.
  2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
  3. Part B consists of 5 Units. Answer any one full question from each unit.
  4. Each question carries 10 marks and may have a, b, c, d as sub questions.

### Part-A

All the following questions carry equal marks (10X2M=20 Marks)

1.	Define lithography.	02
2.	Define Threshold voltage.	02
3.	List the various color coding used in stick diagram	02
4.	Sketch a stick diagram for 2 input NAND gate	02
5.	What is pass transistor logic?	02
6.	What is fan-out of a gate?	02
7.	Write the principle DRAM cell.	02
8.	What is comparator?	02
9.	Define FPGA.	02
10.	Define controllability.	02

### Part-B

Answer All the following questions. (10M X 5=50Marks)

11	a) With neat sketches explain CMOS fabrication using n-well process.	06
	b) Draw CMOS inverter diagram.	04
OR		
12	For nMOS inverter driven by another nMOS inverter, derive the expression for $Z_{pu}/Z_{pd}$ ratio.	10
13	Sketch the circuit schematic, stick diagram and layout of CMOS 2-Input NAND gate.	10
OR		
14	a) Explain with neat diagram explain $\lambda$ - based design rules for transistors, contact cuts and vias.	07
	b) What is the need for design rules?	03
15	a) Write about alternative gate circuits.	05
	b) What is meant by sheet resistance?	05

	OR	
16	a) Describe the sources of wiring capacitance.	05
	b) List the logical constraints of layers.	05
17	a) Draw the logic diagram of zero/one detector and explain its operation with the help of stick diagram.	05
	b) Explain about ALU subsystem.	05
	OR	
18	a) Describe briefly 4-bit parallel adder.	05
	b) Draw and explain the operation of SRAM cell.	05
19	a) Explain the structure and principle of PLA.	05
	b) Explain the architecture of FPGA.	05
	OR	
20	a) What is the need for testing explain with an example?	04
	b) Discuss chip level testing techniques.	06