R20 Regulation *Subject code: 3P6DD*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech VI Semester Supplementary Examinations, February 2024

VLSI DESIGN

(Electronics and Communication Engineering)

Maximum Marks: 70 Duration: 3 hours

Note:
1. This question paper contains two parts A and B.
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit which carries 10M.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks	(10X2M=20 Marks)	CO	Bloom Tx
1	What are main advantages of SOI CMOS technology?	CO1	L1
2	How the potential difference between the source and the body (Vsb) affects the threshold?	CO1	L2
3	Draw the stick diagram and layout for CMOS Inverter.	CO2	L1
4	What are the different MOS layers?	CO2	L1
5	Write about the constraints in choice of layers.	CO3	L1
6	Define Fan-in and Fan-out.	CO3	L1
7	Obtain the critical path delay of 4-bit ripple carry adder and draw the circuit.	CO4	L1
8	Compare SRAM and DRAM.	CO4	L2
9	What is programmable logic array?	CO5	L1
10	List any two faults that occur during manufacturing.	CO5	L1

Part-B

Answer All the following questions.	(5X10M=50Marks)		
11	Draw the fabrication steps of CMOS FET and explain its operation in detail. (10M)	CO1	L2
	OR		
12	Derive the expression for estimation of Pull-Up to Pull-Down ratio of an n-MOS inverter driven by another n-MOS inverter. (10M)	CO1	L4
13	Design an area efficient layout diagram for the CMOS logic shown below. (10M) $Y = \overline{(A+B+C)}$.	CO2	L4
	OR		
14	Explain "2µm Double Metal, Double Poly, CMOS/BiCMOS rules". (10M)	CO2	L2
15	A. What are the alternate gate circuits available? Explain any one of item with a suitable sketch. (5M) B. Implement the realization of NAND & NOR gates using NMOS and PMOS. (5M)	CO3	L2 L2
	OR		

16	A. Describe about the methods for driving large capacitive loads. (5M) B. Discuss the inverter delay and propagation delay. (5M)	CO3	L2 L2
17	Explain about design of an ALU subsystem in brief. (10M)	CO4	L2
	OR		
18	Draw the circuit diagram of 6 T SRAM cell and explain read and write operations. (10M)	CO4	L4
19	A. Implement the following Boolean functions using the PAL device. (5M) $W(A, B, C, D) = \Sigma m(2, 12, 13)$ $X(A, B, C, D) = \Sigma m(7, 8, 9, 10, 11, 12, 13, 14, 15)$ $Y(A, B, C, D) = \Sigma m(0, 2, 3, 4, 5, 6, 7, 8, 10, 11, 15)$ $Z(A, B, C, D) = \Sigma m(1, 2, 8, 12, 13)$ B. Explain Architecture of FPGA in detail. (5M)	CO5	L2 L2
	OR		
20	Why the chip testing is needed? At what levels testing a chip can occur? (10M)	CO5	L2