R20 Regulation *Subject code: 3P5DD*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech V Semester Regular/Supplementary Examinations, February 2024

MICROPROCESSORS AND MICROCONTROLLERS

(ECE)

Maximum Marks: 70 Date:22.02.2024 Duration: 3 hours

Note: **1.This question paper contains two parts A and B.**
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

	Part-A	CO	Bloom Tx
All the following questions carry equal marks (10x2M=20 Marks)			
1	Demonstrate how physical address is generated in 8086.	1	2
2	Define ISR.	1	1
3	Draw the T0 and T1 registers of 8051 microcontroller.	2	2
4	Name and classify the interrupts of 8051 microcontroller.	2	1
5	Give the RS-232 Standard details.	3	3
6	List out the important features of the A/D converter.	3	2
7	Draw the ARM CPSR word format.	4	2
8	What is 'Thumb' in ARM processor.	4	1
9	What are the advantages of OMAP processors.	5	1
10	Write two features of Cortex processors.	5	1
	Part-B		
Answer All the following questions. (5X10M=50Marks)			Bloom Tx level
11	Explain about the minimum mode pin diagram of 8086 microprocessor 10M	1	2
	OR		
12	Explain the architecture of 8086 microprocessor 10M	1	2
13	a. Explain about TCON special function register with a diagram in 8051 microcontroller. 5M	2	2
	b. Explain various addressing modes of 8051 with examples. 5M	2	2
	OR		
14	Draw architecture of 8051 microcontroller and explain in detail. 10M	2	3
15	a. Draw and explain the working of UART 5M	3	2
	b. Explain the interfacing procedure of an 8 - bit DAC with 8051 microcontroller 5M	3	4
	OR		
16	Explain with all necessary sketches to enable intra communications among peripherals using I2C bus. 10M	3	2
17	With the neat block diagram, explain Architecture of ARM core. 10M	4	2

	OR		
18	a. Explain the load store instructions in ARM 5M	4	2
	b. Draw and explain the 3-stage pipelined instruction execution 5M	4	3
19	a) Explain the different applications of CORTEX processor in detail. 3M b) Discuss CORTEX Architecture in detail. 7M	5	4
	OR		
20	List out different classifications of OMAP processor and explain each one type in detail. 10M	5	3