R20 Regulation *Subject code:3E5DA*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech V Semester Regular/Supplementary Examinations, February 2024

DIGITAL DESIGN THROUGH VERILOG HDL

(ELECTRONICS & COMMUNICATION ENGINEERING)

Maximum Marks: 70 Date:27.02.2024 Duration: 3 hours

Note: 1.This question paper contains two parts A and B.
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

	Part-A	CO	Bloom Tx
All the following questions carry equal marks (10x2M=20 Marks)			
1	Indicate the role of HDL in digital design.	CO1	L1
2	Mention data types used in Verilog HDL.	CO1	L2
3	What causes gate delay?	CO2	L1
4	What are the gate primitives available in Verilog?	CO2	L1
5	List the characteristics of continuous assignments.	CO3	L2
6	State why switch level is useful?	CO3	L2
7	Give the two blocks in behavioral Modeling.	CO4	L1
8	Why are test benches important?	CO4	L2
9	Give a note about system Tasks.	CO5	L1
10	What do you understand by compiler directives?	CO5	L2
	Part-B		
Answer All the following questions. (5X10M=50Marks)		CO	BTL
11	Discuss different levels of design description in Verilog with suitable examples. (10M)	CO1	L2
	OR		
12	Explain the following "lexical conventions" with examples. a) White space b) strengths c) strings (3M+3M+4M)	CO1	L2
13	Classify and explain strengths and contention resolution. (10M)	CO2	L2
	OR		
14	Design and verify Full adder using Verilog HDL Gate-level modeling. (10M)	CO2	L5
15	Write down the Verilog code for 4-to-1 multiplexer using logic equation or using conditional operator in data flow modelling. (10M)	CO3	L3
	OR		
16	a) Explain about CMOS switch and Bi-directional switches related to switch level modelling in Verilog HDL. (5M) b) Design and verify a switch level model at the four channel MOS transistor. (5M)	CO3	L5

17	a) Write short notes on non-blocking assignments and blocking assignments.(5M) b) Explain difference between fork and join. (5M)	CO4	L2
	OR		
18	a) Write a Verilog code for half adder using behavioral modelling. (5M) b) Implement a 3:8 decoder using behavioral modelling. (5M)	CO4	L3
19	Demonstrate in detail about the tasks and Functions in System Verilog with examples. (10M)	CO5	L4
	OR		
20	a) Define user defined primitives with their syntax. Give an example of AND gate built using UDPs. (5M) b) Explain about combinational and sequential UDPs (5M))	CO5	L2