



**B.Tech V Semester Supplementary Examinations, February 2024**

**VLSI DESIGN**

(Electronics and Communication Engineering)

Maximum Marks: 70

Duration: 3 Hours

- Note: 1. This question paper contains two parts A and B.  
 2. Part A is compulsory which carries 10 marks. Answer all questions in Part A.  
 3. Part B consists of 10 questions. Answer any 5 questions which carries 12M.  
 4. Each question carries 12marks and may have a, b, c, d as sub questions.

**Part-A**

All the following questions. Each carry equal marks (10x2M=20 Marks)

1	What is body effect?	L1
2	Define figure of merit.	L1
3	Explain different MOS layers.	L2
4	Sketch a stick diagram for CMOS inverter.	L2
5	What is switch logic?	L1
6	What is fan-in of a gate?	L1
7	Draw the circuit diagram of SRAM cell.	L1
8	What is parity generator?	L1
9	Implement Half adder using PAL.	L2
10	What are functionality tests?	L1

**Part-B**

Answer all the following Questions (10MX 5=50Marks)

11	With neat sketches explain CMOS fabrication in an n-well process.	(L3)	[10M]
OR			
12	Explain the operation of NMOS enhancement transistor.	(L2)	[10M]
13	Sketch the schematic, stick diagram and layout for the Boolean expression $Y = (AB + C)'$ .	(L3)	[10M]
OR			
14	a) Explain about scalable design rules.	(L2)	[6M]
	b) Why the design rules should be followed for layout design.	(L2)	[4M]
15	Explain the effect of cascaded inverters in driving large capacitive loads.	(L2)	[10M]
OR			

16	a) Explain the concept of MOSFET as switches. (L2)	[4M]
	b) Derive the expression for time delays in case of MOSFETs. (L3)	[6M]
17	Draw the schematic and explain the operation of 6T SRAM. (L3)	[10M]
OR		
18	a) Explain about serial access memories. (L2)	[5M]
	b) Explain about different types of ROM. (L2)	[5M]
19	Explain the architecture of CPLD with neat diagram.	[10M]
OR		
20	a) Write about CMOS testing. (L1)	[5M]
	b) Explain about design strategies for testing. (L2)	[5M]