Regulation R18 *Subject code: 2E6BB*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech VI Semester Supplementary Examinations, February 2024

Computer Architecture

(EEE)

Maximum Marks: 70 Date:24.02.2024 Duration: 3 hours

Note:
1. **This question paper contains two parts A and B.**
2. **Part A is compulsory which carries 20 marks. Answer all questions in Part A.**
3. **Part B consists of 5 Units. Answer any one full question from each unit which carries 10M.**
4. **Each question carries 10 marks and may have a, b, c, d as sub questions.**

Part-A

All the following questions carry equal marks (10X2M=20 Marks)		CO	Bloom Tx
1	Compare RISC with CISC?	CO1	L3
2	Differentiate between Computer Architecture and Organization	CO1	L3
3	What do you mean by memory hierarchy?	CO2	L1
4	Why does increasing the capacity of cache tend to increase its hit rate?	CO2	L2
5	Write the benefits of serial communication?	CO3	L1
6	What is a priority interrupt?	CO3	L1
7	What is the purpose of PUSH and POP instruction in microprocessor instruction set?	CO4	L1
8	What is the difference between opcode and operand?	CO4	L1
9	Define instruction level of pipelining?	CO5	L1
10	How many segments are there in the pipeline?	CO5	L1

Part-B

Answer All the following questions. (10MX 5=50Marks)			
11	Draw the flow chart of booth's multiplication algorithm in details? [10]	CO1	L3
	OR		
12	A, What is the difference between a hardwired control unit and a micro programmed. [5] B. Explain the multi-bus organization of computer architecture. [5]	CO1	L3 L2
13	What is meant by associative memory? Explain briefly the hardware organization of such a memory. [10]	CO2	L1
	OR		
14	What is virtual memory? Explain the steps involved in virtual memory address translation. [10]	CO2	L2
15	Explain the operation of DMA using a block diagram. Give an example application of DMA data transfer. [10]	CO3	L2
	OR		

16	A. What Bus arbitration and Explain approaching methods? [5] B. Discuss about interface circuits and Explain parallel port? [5]	CO3	L1 L2
17	Explain the architecture of 8086 microprocessors with neat block diagram?[10]	CO4	L2
	OR		
18	Explain memory segmentation in 8086 microprocessors? What are the advantages and disadvantages? [10]	CO4	L2
19	What do you understand by Instruction Pipeline? Mention the stages of Pipeline. [10]	CO5	L2
	OR		
20	Explain the features of VLIW Architecture, advantages and disadvantages with neat block diagram. [10]	CO5	L2