R20 Regulation *Subject code:3P3FA*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A' Grade)

B.Tech III Semester Regular/Supplementary Examinations, March/April 2023

Digital Logic Design

(IT)

Maximum Marks: 70 Date:01.04.2023 Duration: 3 hours

Note: 1.This question paper contains two parts A and B.
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks (10x2M=20 Marks)

1 Why we need a data representation system?
2 Perform the conversion $(7777)_8 = (?)_{10} = (?)_2$
3 For the given logic equation, implement with three NOR gates Y=(A+B).(C+D)
4 What is k map? How it is different from truth table.
5 Realize OR function using 2:1 MUX
6 Draw the logic diagram of a one to four line demultiplexer.
7 Differentiate between RING and RIPPLE counter.
8 Why S=R=1 is not permitted in SR flipflop
9 What is the need for state reduction in sequential circuit design?
10 Compare Mealy and Moore models.

Part-B

Answer All the following questions. (5X10M=50Marks)

11 A. Perform the subtraction with the binary number 11010 – 1101 using (i) 2's complement method (ii) 1's complement method 5M
B. Compare the BCD code and Gray code. 5M

OR

12 How a Hamming code locate the error? Explain with an example. 10M

13 A. What is Boolean algebra? How it is different from normal algebra? why it is specially suited to logic? 5M
B. How can you get a Boolean expression from a truth table? Explain with an example. 5M

OR

14 Simplify the expression by using K-Map method
$f(A,B,C,D) = \Sigma m(1,2,5,6,7,9,10) + \Sigma d(0,13,15)$ 10M

15 Design 4-bit GREY to BCD code converter using logic gates. 10M

OR

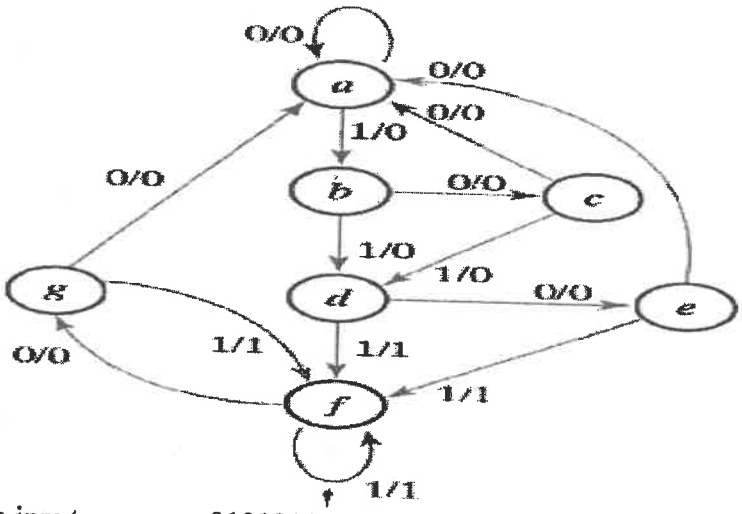
16 Implement a function $F(A,B,C,D) = \Sigma m(0,1,3,4,8,9,15)$ using multiplexer 10M

17 Show the T flip flop implementation from SR flip flop and JK flip flop. 10M

OR

18 Describe the operation of shift register. Discuss different methods of entering data into the register and reading it. 10M

19 10M



An input sequence 01010110100 is applied to a sequential circuit. Draw the state diagram and table then reduce it.

OR

20 Explain the capabilities and limitations of FSM. 10M