R20 Regulation *Subject code:3P3DB*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A' Grade)

B.Tech III Semester Regular/Supplementary Examinations, March/April 2023

DIGITAL LOGIC DESIGN

(ECE)

Maximum Marks: 70 Date:01.04.2023 Duration: 3 hours

Note: 1.This question paper contains two parts A and B.
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks (10x2M=20 Marks)

1 Find the 2's complement and 1's complement of binary number (101101)
2 Convert the binary number (1101100010011011) into hexadecimal number.
3 What are the universal gates? Why they called as universal gates?
4 What are the De Morgan's theorems?
5 Draw the basic circuit of half adder and mention the truth table
6 Define the Multiplexer.
7 What is the difference between Latch and Flip flop?.
8 What is the characteristic equation of D and T flip flop?
9 Define finite state machine
10 List the limitations of finite state machines

Part-B

Answer All the following questions. (5X10M=50Marks)

11 A. Convert the hexadecimal number 68BE to binary and then from binary convert it to octal 5M
B. Convert the following to Decimal then to Octal 5M
a) $(125F)_{16}$ b) $(10111111)_2$

OR

12 A. What is a Binary Coded Decimal? Explain its properties. 5M
B. Explain how to convert from binary to hexadecimal number with an example. Mention the advantages of hexadecimal system. 5M

13 A. Implement AND,OR and NOR by using NAND gate. 5M
B. Simplify the following Boolean function using three variable maps. 5M
$F(x,y,z) = \sum(0,2,6,7)$

OR

14 A. Show that the dual of the exclusive OR is also its compliment. 5M
B. Demonstrate by means of truth tables the Boolean Associate law and Distributive law 5M

15	Design the Full adder and draw the logic diagram.	10M
	OR	
16	Explain about Decoder and implement the 4x16 Decoder.	10M
17	A. Draw the block diagram of asynchronous sequential circuit. Explain.	5M
	B. Explain the operation of 4 bit binary counter	5M
	OR	
18	A. What is a sequential circuit ? Explain the Latch using NOR gate.	5M
	B. Using D flip flops and wave forms explain the working of a 4bit SISO shift register.	5M
19	With a neat block diagram, explain the Moore model of clocked sequential circuit.	10M
	OR	
20	A. What are the capabilities of Finite State Machine ? discuss.	5M
	B. Write the differences between Mealy and Moore machines.	5M