R18 Regulation *Subject code: 2P3EC*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A' Grade)

B.Tech III Semester Supplementary Examinations, March/April 2023

DIGITAL LOGIC DESIGN
(COMPUTER SCIENCE & ENGINEERING)

Maximum Marks: 70 Date:01.04.2023 Duration: 3 hours

Note: 1.This question paper contains two parts A and B.
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit which carries 10M.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks **(10x2M=20 Marks)**

1 Convert (67A9)16 into decimal.
2 What are 2's complement and 9's complement of a numbers? Give examples.
3 Differentiate multiplexer and de-multiplexer
4 Draw the logic circuit of a full adder and give its truth table.
5 Differentiate between Latch and flip flop.
6 Draw the logic diagram of a master slave J-K flip-flop.
7 Explain about sequential programmable logic devices
8 List various Addressing Modes in 8086 MIcrprocessor
9 Differentiate between RAM and ROM.
10 Why programmable AND gates are used in PLA instead of a decoder.

Part-B

Answer All the following questions. **(5X10M=50Marks)**

11 A. i) Convert (657)8 into decimal. ii) Convert (2348)10 into hexa decimal.
B.Represent the decimal number 46.5 as a floating point number with 16 bit mantissa and 8 bit exponent. (5+5)

OR

12 Simplify the following Boolean expressions to a minimum number of literals
(i) ABC+A'B+ABC' (ii) xy + x(wz+wz') (10M)

13 A. Simplify the following Boolean functions, using a four variable Karnaugh map method and implement the simplified function using NAND gates
$F(A,B,C,D) = \Sigma 0,2,4,5,6,7,8,10,13,15)$
B. Show that the dual of the exclusive OR is also its compliment. (5+5)

OR

14 Derive and Implement Exclusive OR function involving three variables using only NAND function. (10M)

15 Realize a full subtractor using decoders (10M)

OR

16 A. Design half adder using only NAND gates.

B. Design a combinational circuit which converts BCD to Excess-3 code. (5+5)

17 Explain the all assembler directives of 8086 with suitable examples. (10M)

OR

18 A. Draw and explain the each bit of flag register of 8086 family microprocessor.
B. Describe the implementation of pipelined process of 8086. (5+5)

19 With a neat diagram explain in detail about two dimensional memory decoding scheme. (10M)

OR

20 Explain about RAM and ROM in detail. (10M)