Regulation R20 *Subject code:* 3E7DA

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A+' Grade)

B.Tech VII Semester Supplementary Examinations, April 2024

ANALOG IC DESIGN

(Electronics and Communication Engineering)

Maximum Marks: 70 Date:25.04.2024 Duration: 3 hours

Note: **1.This question paper contains two parts A and B.**
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks (10X2M=20 Marks)

1 What is body effect?

2 What is sheet resistance?

3 What is the working principle of current mirror?

4 What is the need of voltage reference?

5 Classify output amplifiers.

6 What is current amplifier?

7 Define Slew rate.

8 Give the steps in designing typical CMOS Op-amp.

9 Draw the model for ideal comparator.

10 Draw the circuit symbol for ideal comparator.

Part-B

Answer All the following questions. (5X10M=50Marks)

11 Draw the small-signal model for the MOS transistor. Briefly explain each component in that. [10]

OR

12 Discuss about the Passive Components of the MOS transistor. [10]

13 Write short notes on current sinks and sources. [10]

OR

14 Discuss about current and voltage references and band gap reference in detail with suitable diagrams. [10]

15 List different types of inverting CMOS amplifiers and explain any one of it. [10]

OR

16 Describe small signal model of CASCODE Amplifiers. [10]

17 Explain about the design of CMOS op amps. [10]

OR

18 Derive the expression for power-supply rejection ratio of two-stage op-amps. [10]

19 Explain about the different types of Open loop comparators. [10]

OR

20 Explain the auto zeroing concept of improving the performance of a comparator. [10]