R20 Regulation *Subject code:3P5DD*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A' Grade)

B.Tech V Semester Regular Examinations, January 2023

MICROPROCESSORS AND MICROCONTROLLERS

(Electronics and Communication Engineering)

Maximum Marks: 70 Date:18.01.2023 Duration: 3 hours

Note: 1.This question paper contains two parts A and B.
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit which carries 10M.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks (10x2M=20 Marks)

1 List out the available clock rates of 8086 microprocessor.

2 Write the functions of AX, BX, CX and DX registers.

3 List out the main features of 8051 microcontroller?

4 What is the size of on chip RAM and ROM of 8051?

5 What is the purpose of 8255 PPI?

6 What is UART?

7 Write examples for ARM data transfer instructions?

8 What is the load-store architecture feature of ARM.

9 Mention major application areas of OMAP processor

10 Write the features of CORTEX Processor.

Part-B

Answer All the following questions. (5X10M=50Marks)

11 A. Describe the various addressing modes of 8086 microprocessor with examples.
B. Assume 8086 being operated in minimum mode. Describe the function of the following pins in minimum mode: i) MN/MX ii) HOLD and HLDA iii) DEN iv) ALE. [5+5]

OR

12 Write an assembly language program to perform multiplication of two 16-bit numbers. [10]

13 A. Illustrate the memory organization of 8051microcontroller with neat sketches.
B. Define the each bit field of the IE and TMOD registers in 8051. [5+5]

OR

14 A. Draw the architecture of 8051 microcontroller and discuss each section.
B. Write 8051 program to generate 1 kHz square wave on pin P1.1 of port 1 using Timer interrupt. [5+5]

15 A. Describe the various modes of operations for 8255 PPI using relevant neat diagrams.
B. Differentiate between asynchronous and synchronous data transfer schemes. [5+5]

OR

16 A. Explain the control word format of 8255 in I/O and BSR mode.
B. Compare the 2C versus SPI interface. [5+5]

17 A. Discuss the key features of the ARM Architecture.
B. Illustrate the functionality of Branch & Load Instructions using simple examples. [5+5]

OR

18 A. Illustrate the Pipeline concept in ARM processor using neat sketches.
B. Discuss the ARM Data processing instructions set with examples. [5+5]

19 Explain the architecture of ARM Cortex processor with the help of a neat block diagram. [10]

OR

20 A. Illustrate Shift and Rotate instructions available in ARM Cortex-M3 instruction set with an example.
B. Draw block diagram for OMAP processor and discuss the each block. [5+5]