R20 Regulation *Subject code:3E5DA*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A' Grade)

B.TechV Semester Regular Examinations, January 2023

DIGITAL DESIGN THROUGH VERILOG HDL

(Professional Elective)

(Electronics and Communication Engineering)

Maximum Marks: 70 Date:23.01.2023 Duration: 3 hours

Note: 1.This question paper contains two parts A and B.
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit which carries 10M.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks (10x2M=20 Marks)

1 Define Keywords and Identifiers.
2 What do you mean by Module Path.
3 Define strengths and content resolution.
4 Describe array of instances of primitives.
5 What is Continuous Assignment Structure?
6 How is Procedure Assignment characterized?
7 What do you mean by Multi-Way Branching.
8 Draw a 2 to 4 decoder using enable and write the design module in behavioral model.
9 Define Path Delay.
10 Define Compiler Directives.

Part-B

Answer All the following questions. (5X10M=50Marks)

11 A. Explain port declaration with an example using Verilog code. [5]
B. Explain the Strings with suitable Example. [5]

OR

12 A. Explain in detail the levels of Design Description [5]
B. Write about white space characters and variables with examples. [5]

13 Design 1:8 demultiplexer using gate level modelling. [10]

OR

14 Write the Verilog code for 4 X1 Multiplexer using the tristate buffer in the gate level modelling. [10]

15 Design half adder using CMOS switches. [10]

OR

16 A. Write short notes on time delays with switch primitives relevant to switch level modelling. [5]
B. Write a Verilog HDL code for n-bit right-to-left shift register using data flow level. [5]

17 Discuss the following related to behavioural level modelling with necessary syntax and example. (i) Block statement (ii) Case statement [5+5]

OR

18 A. Explain blocking and non-blocking statement with examples. [5]
B. What is the difference between a sequential block and a parallel block? Explain using an example. Can a sequential block appear with in a parallel block? [5]

19 Define parameter and explain any combinational circuit using parameter keyword. [10]

OR

20 A. Design Verilog module using Path Delay. [5]
B. Define user defined primitives with their syntax. Give an example of 4 to 1 multiplexer built using UDPs. [5]