Regulation R18 *Subject code: 2P5DB*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A' Grade)

B.Tech V Semester Supplementary Examinations, January 2023

VLSI DESIGN

(Electronics and Communication Engineering)

Maximum Marks: 70 09-01-2023 **Duration: 3 Hours**

Part-A

All the following questions. Each carry equal marks (10x2M=20 Marks)

1 What is body effect?
2 Define figure of merit.
3 Explain different MOS layers.
4 Sketch a stick diagram for CMOS inverter.
5 What is switch logic?
6 What is fan-in of a gate?
7 Draw the circuit diagram of SRAM cell.
8 What is parity generator?
9 Implement Half adder using PAL.
10 What are functionality tests?

Part-B

Answer all the following Questions (5X10M=50Marks)

11. Explain NMOS fabrication process. [10M]

OR

12 Explain the operation of NMOS enhancement transistor. [10M]

13 Sketch the schematic, stick diagram and layout for the Boolean expression Y = (B + AC)'. [10M]

OR

14 a) Explain about scalable design rules. [6M]

b) Why the design rules should be followed for layout design. [4M]

15 Explain the effect of cascaded inverters in driving large capacitive loads. [10M]

OR

16 a) Explain the concept of MOSFET as switches. [4M]

b) Derive the expression for time delays in case of MOSFETs. [6M]

17 Draw the schematic and explain the operation of Wallace tree Multiplier. [10M]

OR

18 a) Explain about serial access memories. [5M]

b) Explain about different types of ROM. [5M]

19 Explain the architecture of CPLD with neat diagram. [10M]

OR

20 a) Write about CMOS testing. [5M]

b) Explain about design strategies for testing. [5M]