R20 Regulation *Subject code:* 3P3FA

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A' Grade)

B.Tech III Semester Regular Examinations, February 2022

DIGITAL LOGIC DESIGN

(Information Technology)

Maximum Marks: 70 Date:23.02.2022 Duration: 3 hours

Note: 1.This question paper contains two parts A and B.
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks (10x2M=20 Marks)

1 Show that $(X + Y' + XY)(X + Y')(X'Y) = 0$
2 Binary to Decimal conversion : $(111001.1011)_2$
3 List the methods adopted to reduce Boolean function?
4 What are called don't care conditions?
5 Differentiate combinational and sequential circuits.
6 Define Encoder?
7 What are the types of shift register?
8 List the two models in sequential circuits.
9 Define the state table and state diagram.
10 Define race condition.

Part-B

Answer All the following questions. (5X10M=50Marks)

11 Two numbers A & B in Hex are given A= 85CA, B= 23C6
i. Find the Decimal equivalent of A & B ii. Find the binary of A & B [10]
iii. What is the sum of A& B in HEX

OR

12 a) Write down the 1's and 2's complement of the following numbers.
i. – 4 ii. +253 iii. – 181 [5]
b) Determine the Hamming code for the information 1011, with even parity. [5]

13 Find a minimum sum of products expression for the following function using Quine McClusky method. [10]
$F (A,B,C,D,E) = \sum(0,2,3,5,7,9,11,13,14,16,18,24,26,28,30)$

OR

14 Given the Boolean function
$F = xy'z + x'y'z + w'xy + wx'y + wxy$ [10]
a) Obtain the truth table of the function.
b) Draw the logic diagram using the original Boolean expression.
c) Simplify the function to a minimum number of literals using Boolean algebra.
d) Obtain the truth table of the function from the simplified expression and show that it is the same as the one in part (a)
e) Draw the logic diagram from the simplified expression and compare the total number of gates with the diagram of part (b)

15 Design a half adder. What is the limitation of half adder? How do you convert it into a Full-Adder? [10]

OR

16 Narrate the combinational circuit design procedure with Examples. [10]

17 a) Define SR–Flip-flop with the help of a logic diagram and characteristic table? [5]
b) Convert a T-FF into an S-R FF. Draw the circuit. [5]

OR

18 Design a counter with the sequence 0,1,3,7,6,4,0. [10]

19 Draw and explain the state transition diagram of mod-6 counter in a asynchronous sequential logic. [10]

OR

20 Explain about Mealy machine with an example. [10]