R20 Regulation *Subject code: 3P3DB*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A' Grade)

B. Tech III Semester Regular Examinations, February 2022

DIGITAL LOGIC DESIGN

(ELECTRONICS & COMMUNICATION ENGINEERING)

Maximum Marks: 70 Date:22.02.2022 Duration: 3 hours

Note: 1. This question paper contains two parts A and B.
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks (10x2M=20 Marks)

1 Convert $(115)_{10}$ and $(235)_{10}$ into hexadecimal numbers.
2 Analyze the octal and hexadecimal equivalent of $(377)_{10}$.
3 State De-Morgan's theorem.
4 Define 'Minterm' and 'Maxterm' with an example.
5 Distinguish between half subtractor and full subtractor.
6 Draw full adder using two half adders.
7 Generalize the differences between combinational and sequential circuits.
8 Write the truth table for JK Flip flop.
9 Write the differences between Mealy and Moore circuits.
10 Write the role of master clock generator in synchronous circuits.

Part-B

Answer All the following questions. (5X10M=50Marks)

11 Explain in detail about error detecting and error correcting code. [10]

OR

12 (a) Convert $(725.25)_8$ to its decimal, binary and Hexadecimal equivalent. [5]
(b) Find 1's and 2's Complement of 8-digit binary number 10101101. [5]

13 Using K-map method, Reduce the following Boolean function $F=\Sigma m\,(0,2,3,6,7) + d\,(8,10,11,15)$ and obtain minimal SOP. [10]

OR

14 Given that a frame with bit sequence 1101011011 is transmitted, it has been received as 1101011010.Examine the method of detecting the error using any one error detecting code. [10]

15 Find the Boolean expression of 2 to 4 decoder & 3 to 8 decoder and draw the logic diagram from the truth table. [10]

OR

16 Demonstrate on a 2-bit magnitude comparator with three outputs: A>B, A=B and A<B. [10]

17 Determine the state table, characteristic table and an excitation table for D Flip Flop. [10]

OR

18 Explain the working principle of JK FF and concept of Master/Slave JK FF. [10]

19 Discuss about a 3 bit (MOD 8) Synchronous UP/Down counter with neat state diagram, state table, excitation table, K-map simplification and its circuit diagram. [10]

OR

20 Develop a state table, characteristic table and an excitation table for SR Flip Flop. [10]