Regulation R18 *Subject code: 2E8DE*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A' Grade)

B.Tech. VIII Semester Supplementary Examinations, April 2023

DESIGN OF FAULT TOLERANT SYSTEMS

(ELECTRONICS & COMMUNICATION ENGINEERING)

Maximum Marks: 70 Date:05.05.2023 Duration: 3 hours

Note: 1.This question paper contains two parts A and B.
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit which carries 10M.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks (10x2M=20 Marks)

1 Define Reliability.
2 Compare failures to faults?
3 What is the need for Totally Self Checking Checkers?
4 What is Fail safe Logic?
5 List out the design procedures involved in use of control Logic.
6 Define Observability with neat diagram.
7 Define the types of BIST.
8 How do you define BEST?
9 What are *User-Defined Registers*?
10 Write about *One Serial Scan chain*

Part-B

Answer All the following questions. (5X10M=50Marks)

11 a) How do the terms Fault, Error and Failure are discriminated. Explain with appropriate examples.
b) A computer system contains 10,000 components each with failure rate 0.5% per 1000 hours. What is the period of 0.99 reliability of this system? [6+4]M

OR

12 Explain in detail about Time redundancy and Software redundancy schemes. [10M]

13 Design fail-safe synchronous sequential machine for a given machine A using Berger codes. Machine A is: [10M]

Present state	Input	
	x=0	x=1
A	E,0	B,0
B	C,0	D,0
C	A,0	D,0
D	E.0	D,1
E	A,0	D,1

OR

14 Explain the operation of "The Two-rail-Checker" with appropriate example. [10M]

15 Derive the Reed-Muller circuit for $f=WX+WY+XY$. [10M]

OR

16 Discuss with example Design of Testable Combinational logic Circuits,using Syndrome-testable design and list out the Drawbacks. [10M]

17 As related to BIST, Explain BIST Types. [10M]

OR

18 Explain in detail about the factors involved in designing a BIST. [10M]

19 What do you understand by Board Level scan chain structures? Explain various arrangements involved in it in detail. [10M]

OR

20 Write in detail about TAP controller. [10M]