



Regulation: R17

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY
(Autonomous, Accredited by NAAC with 'A' Grade)

Subject code: 1E6DC

B.Tech. III Year II Semester Supplementary Examinations, June 2022
DIGITAL SYSTEM DESIGN
(Electronics & Communication Engineering)

Maximum Marks: 70

Duration: 3 hours

- Note:
1. This question paper contains two parts A and B.
 2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
 3. Part B consists of 5 Units. Answer any one full question from each unit.
 4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks (10x2M=20 Marks)

- 1 Define State Incompatibility.
- 2 Explain about FSM.
- 3 What are the types of ROM?
- 4 Explain about Multiplexer.
- 5 Write the basic components of ASM Charts.
- 6 What is binary multiplexer?
- 7 Write about Fault equivalence and fault location
- 8 Explain about Kohavi algorithm in Digital Circuits.
- 9 What is mean by Circuit Test Approach?
- 10 Explain about Machine identification in Digital Circuits.

Part-B

Answer All the following questions.

(10M X 5=50Marks)

- 11 Explain about **Merger Table and Merger Graph** methods and reduce the incompletely specified machine whose state table is shown below Table using **Merger Table and Merger Graph**.

P.S	N,S,Z			
	00	01	11	10
A	E,0	--	--	--
B	--	F,1	E,1	A,1
C	F,0	--	A,0	F,1
D	--	--	A,1	--
E	--	C,0	B,0	D,1
F	C,0	C,1	--	--
G	E,0	--	--	A,1

OR

- 12 a). Explain Mealy machine with appropriate block diagram.
b). Give the capabilities of FSM.
- 13 a). What are the various programmable logic devices? Compare them.

b). Implement the following Boolean functions using PAL
 $F1(X, Y, Z) = \sum(1, 2, 4, 6)$ $F2(X, Y, Z) = \sum(0, 1, 6, 7)$
 $F3(X, Y, Z) = \sum(2, 6)$

OR

- 14 a). Explain and draw the circuit diagram of BCD Adder. Add two numbers 8 and 4 in BCD Addition.
- b). Explain the types of ROM's.
- 15 a). What are the basic blocks in ASM Charts. Explain with an example.
- b). Explain about implementation of Binary Multiplier circuit.

OR

- 16 a). Draw the portion of an ASM chart that specify a conditional operation to increment register(r) during state t1 and transfer to state t2 if control inputs z and y are equal to 1 and 0 respectively.
- b). Explain about Realization of SM charts.
- 17 a). Explain the Boolean difference method with an example.
- b). Explain PODEM with an example.

OR

- 18 A two level AND-OR circuit has four AND gates feeding one OR gate. The four AND gates realize the product terms $x_1x_3x_4$, x_2x_4 , $x_1'x_3'x_4'$, $x_1x_2x_3$ respectively. Derive 'a' test & 'b' tests for detecting multiple stuck at faults.
- 19 a). Explain the procedure of designing a fault detection experiment with the help of an example.
- b). Explain the procedure for identifying the initial and final states of a Sequential machine using an example.

OR

- 20 Explain the procedure of designing a fault detection experiment for a Sequential Circuit using an example.