R18 Regulation *Subject code: 2P5DB*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A' Grade)

B.Tech V Semester Regular/Supplementary Examinations, December 2021

VLSI DESIGN

(Electronics and Communication Engineering)

Maximum Marks: 70 ***Date: 03.01.2022*** Duration: 3 hours

Note: 1.This question paper contains two parts A and B.
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks (10x2M=20 Marks)

1 What is MOS?
2 What is pull UP?
3 Write down the advantages of Stick Diagram?
4 Write design rules for CMOS?
5 What are the Logic Gates?
6 What is Wiring Capacitance?
7 What is Parity Generators?
8 What is ROM?
9 Why Testing is need?
10 What are the Standard Cells?

Part-B

Answer All the following questions. (5X10M=50Marks)

11 a) Explain CMOS Inverter with V-I characteristics? (5M)
b) Differentiate the BJT and CMOS technologies? (5M)

OR

12 a) Write the relationship between I_{ds} -$V_{ds.}$ (7M)
b) Explain MOS Transistor threshold voltage, g_m and g_{ds}? (3M)

13 a) Draw the diagram of NAND gate using CMOS Inverter? (5M)
b) Explain Scaling MOS circuits? (5M)

OR

14 a) Explain VLSI Design flow and MOS Layers. (5M)
b) Explain Contacts and Transistor layout? (5M)

15 a) Explain Logic gates and Other complex gates? (5M)
b) Explain switch logic and Alternate Gate circuits? (5M)

OR

16 a) Explain Driving large capacitive loads? (5M)
b) Explain the Fan-in and Fan out? (5M)

17 a) Discuss about subsystem Design? (3M)
b) Explain about 4-bit Carry look ahead adder? (7M)

OR

18 Explain SRAM and DRAM? (10M)

19 a) Explain Programmable Array Logic? (5M)
b) What are the parameters influencing low power design? (5M)

OR

20 a) Explain CMOS Testing? (5M)
b) Explain Chip level Test Technique? (5M)