Regulation R17 *Subject code: 1P5DB*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A' Grade)

B.Tech III Year I Semester Supplementary Examinations, December 2021

LINEAR & DIGITAL IC APPLICATIONS

(Electronics and Communication Engineering)

Maximum Marks: 70 ***Date:29.12.2021*** Duration: 3 hours

Part-A

All the following questions carry equal marks (10x2M=20 Marks)

1 What is slew rate?
2 List features of 741 op-amp.
3 Write the relation between lock range and capture range in a PLL.
4 Draw the frequency response characteristics of a notch filter.
5 What do you mean by quantization error in an ADC?
6 Mention the advantages of R-2R ladder DAC.
7 Define noise margin and propagation delay.
8 Discuss about parity generator/checker IC.
9 What is race around condition? How is it avoided?
10 List the basic types of shift registers in terms of data movement.

Part-B

Answer All the following questions. (5X10M=50Marks)

11.a Explain various DC and AC characteristics of an op-amp. (5M)
b. Determine the output voltage of the differential amplifier having input voltages V1=1mV and V2=2 mV. The amplifier has a differential gain of 5000 and CMRR 1000. (5M)

OR

12. Explain the operation of Integrator and plot its output waveforms for different inputs. (10M)

13 Explain triangular waveform generator using IC 741 and derive frequency of oscillations. (10M)

OR

14.a Draw the block diagram of 565 PLL and explain about each block. (5M)
b Calculate output frequency f0 , lock range and capture range of a 565 PLL if RT = 10K ohms, CT = 0.01μF and C = 10 μF. (5M)

15.a With neat diagram explain working of weighted resistor DAC. (5M)
b Compare weighted resistor DAC and R-2R ladder DAC. (5M)

OR

16.a Explain the working of a parallel comparator type A/D converter. (5M)
b Write the specifications of ADC. (5M)

17.a Design BCD to gray code converter. (5M)

b Design 16-bit comparator using 74LS185 IC. (5M)

OR

18 Explain with neat diagram interfacing of TTL gate driving CMOS and CMOS driving TTL Gates. (10M)

19 Differentiate between ripple counter and synchronous counter? Design a 3- bit synchronous counter. (10M)

OR

20.a Draw and explain 4-bit universal shift register. (5M)

b Design a Modulo-12 ripple counter using 74×74. (5M)