Regulation *R17* *Subject code:1E5DE*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A' Grade)

B.Tech III Year I Semester Supplementary Examinations, December 2021

DIGITAL DESIGN THROUGH VERILOG HDL

(Electronics and Communication Engineering)

Maximum Marks: 70 Date:08.02.2022 Duration: 3 hours

Note: 1.This question paper contains two parts A and B.
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks (10x2M=20 Marks)

1 Explain simulation and synthesis with differences.
2 What are the basic logic values available in Verilog HDL?
3 Write a Verilog code for half adder?
4 Define gate delays with example.
5 Write about Bitwise operators in Verilog?
6 Write about bidirectional gates?
7 Write the syntax of event construct?
8 Write a Verilog module for 2 to 4 decoder using case statement?
9 Write about $display task?
10 Write a simple UDP table for 2 input AND gate

Part-B

Answer All the following questions. (5X10M=50Marks)

11 a) Explain levels of design description. (6M)

b) Differentiate between vectors and memories. (4M)

OR

12 a) Explain the following "lexical conventions" with examples. (6M)
(i) key words (ii) identifiers (iii) Numbers

b) Explain about data types in Verilog. (4M)

13 Design and draw the full adder in using basic logic primitives. (10M)

OR

14 Write the Verilog code for 16:1 Multiplexer using the tri-state buffer in the gate level modeling.

15 a) Explain about operators in Verilog. (5M)
b) Design CMOS switch of parallel combination. (5M)

OR

16 Design two-input NAND gate in switch level modeling and write the Verilog code? (10M)

17 a) Explain case construct with an example. (5M)

b) Differentiate between blocking and non-blocking statements in behavioral model. (5M)

OR

18 a) Design 8:1 multiplexer using if else construct. (5M)

b) Explain clocked JK flip flop Verilog module and test bench. (5M)

19 a) Briefly explain combinational UDPs in Verilog. (5M)

b) Differentiate between tasks and Functions. (5M)

OR

20 Explain about sequential UDPs with an example. (10M)