R18 Regulation *Subject code:2P4EB*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A' Grade)

B.Tech IV Semester Regular/Supplementary Examinations, July 2021

COMPUTER ORGANIZATION

(COMPUTER SCIENCE & ENGINEERING)

Maximum Marks: 70 Date:15.07.2021Duration: 3 hours

Note: 1.This question paper contains two parts A and B.
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit which carries 10M.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks **(10x2M=20 Marks)**

1 List out the typical logical and bit manipulation instructions.
2 Define micro program.
3 Contrast 8086 minimum mode with maximum mode?
4 Briefly explain special processor activities?
5 Write about I/O Bus Vs Memory Bus?
6 Explain overflow and underflow?
7 Define miss penalty for cache memory.
8 Differentiate SRAM and DRAM?
9 Write the advantages of pipelining?
10 Draw the system bus structure for multiprocessors.

Part-B

Answer All the following questions. **(10MX 5=50Marks)**

11 A. Give a brief note on instruction cycle. (5M)
B. Compare and Contrast the Computer Design and Computer Architecture. (5M)

OR

12 A. List and explain the functional units of a computer. (6M)
B. Compare hardwired control with microprogrammed control. (4M)

13 A. Draw and explain the 8086 Processor Architecture. (7M)
B. Explain interrupt cycle of 8086? (3M)

OR

14 A. Discuss the physical memory organization? (5M)
B. Explain the register organization in 8086? (5M)

15 Write about DMA function with neat diagram. (10M)

OR

16 A. Show the step-by-step multiplication process using Booth algorithm when the following binary numbers are multiplied. (+33) × (-12). (6M)
B. Calculate the number of characters per second can be transmitted over 1200-baud line in each of the following modes?
i. Synchronous serial transmission.
ii. Asynchronous serial transmission with two stop bits. (4M)

17 A. Give a neat sketch that illustrates the components in a typical memory hierarchy. (5M)

B. Write about Memory Management Hardware. (5M)

OR

18 A. Explain the set-associative mapping of cache memory. (5M)

B. Describe virtual memory in detail. (5M)

19 A. Explain arithmetic pipeline with example. (5M)

B. What are the various forms available for establishing an interconnection network in a multi processor system? (5M)

OR

20 A. Does pipelining get affected by data dependencies among the instruction? Justify your answer with lucid examples. (5M)

B. Explain various Interconnection Structures. (5M)