R18 Regulation *Subject code:2P4BB*

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A' Grade)

B.Tech IV Semester Regular/Supplementary Examinations, July 2021

DIGITAL LOGIC DESIGN

(ELECTRICAL AND ELECTRONICS ENGINEERING)

Maximum Marks: 70 Date:15.07.2021 Duration: 3 hours

Note: **1.This question paper contains two parts A and B.**
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit which carries 10M.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks **(10x2M=20 Marks)**

1 Give the Hexadecimal equivalent of $(5462)_{10}$.

2 Implement the following Boolean function with basic gates.

F= A (B +CD) +BC'

3 Write down the need of K-map?

4 Design a one-bit comparator?

5 Write the difference between Latch and Flipflop with an example?

6 Write the Excitation table and Characteristic equation of T Flipflop?

7 Implement the following function using PAL: F1=Σ(1,4,6,7)

8 Design 3.bit Ring Counter?

9 Write the capabilities and Limitations of Finite State Machines?

10 Differentiate Mealy and Moore machine with an example?

Part-B

Answer All the following questions. (10MX 5=50Marks)

11 A.Reduce the expression using Boolean algebra $A+B\left((A+C)\left(B+\bar{C}\right)D\right)$ (4 Marks)

B.Using Boolean algebra techniques, simplify the given expression: (6 Marks)

i. $C(A+B)+A(B+C)+B(B+C)$

ii. $ABC+A\bar{B}\bar{C}+\bar{A}\bar{B}\bar{C}+A\bar{B}C+ABC$

OR

12 A.Convert the following numbers: (6 Marks)

i. $(B2F8)_{16}$ to Decimal

ii. $(632.97)_{10}$ to Octal

iii. $(0.11011)_2$ to Decimal

B.Obtain the minimal POS expression for $\pi_M(0, 1, 2, 4, 5, 6, 9, 11, 12, 13, 14, 15)$ and implement it in NOR logic?

(4 Marks)

13 Simplify the Boolean function F(w, x, y, z) = Σ(1, 3, 7, 11, 15)Σd(0, 2, 5) and obtain all Prime Implicants and Essential Prime Implicants using Tabulation method. (10 Marks)

OR

14 A. Implement the logic expression given below using (6 Marks)
F = ∑m (0, 1, 3, 5, 8, 11, 12, 14, 15)
i. 8:1 MUX
ii. 16:1 MUX

B. Implement a four bit Adder circuit and explain its operation (4 Marks)

15 Convert the following Flip-Flop conversions. (10 Marks)
i. D flip-flop to T flip-flop
ii. SR flip-flop to JK flip-flop

OR

16 A. Draw the timing waveform and obtain the characteristic equation of (6 Marks)
i. SR Flip Flop
ii. D Flip Flop

B. Explain with timing waveforms "Race around condition" in a Flip-Flop? (4 Marks)

17 A. Draw the Logic diagram of Parallel In, Serial Out Shift Register and explain its operation? (5 Marks)

Design Mod-6 Asynchronous Counter using T Flipflop? (5 Marks)

OR

18 A.Differentiate with appropriate diagrams for the following PLD's: ROM, PLA and PAL? (5 Marks)

B.Explain the working of a 3-bit Synchronous Up counter with a neat logic diagram and functional table? (5 Marks)

19 A.Analyze all the models of Synchronous Sequential circuits? (5 Marks)

B.Differentiate between Partition technique and Merger Chart method with an example? (5 Marks)

OR

20 Obtain the set of maximal compatibles for the sequential machines whose state table is given below using Merger table method (10 Marks)

PS	NS, Output		
	I1	I2	I3
A	C,0	E,1	--
B	C,0	E,-	--
C	B,-	C,0	A,-
D	B,0	C,0	E,-
E	--	E,0	A,-