R17 Regulation *Subject code:* 1P4EA

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A' Grade)

B.Tech II Year II Semester Supplementary Examinations, July 2021

COMPUTER ORGANIZATION

(CSE)

Maximum Marks: 70 Date:18.07.2021 Duration: 3 hours

Note: **1.This question paper contains two parts A and B.**
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit which carries 10M.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks **(10x2M=20 Marks)**

1 Define the basic computer architecture?
2 Write down the the different phases of instruction cycle?
3 Write down the major components of a CPU?
4 What is an assembler directive? Give an example of assembler directive?
5 What is an assembler?
6 What is an interrupt? Mention any two hardware interrupts?
7 Explain overflow and underflow.
8 Differentiate control command and status command?
9 What is cache coherence.
10 Differentiate isolated I/O and memory mapped I/O.

Part-B

Answer All the following questions. **(5X10M=50Marks)**

11 a) List and explain different performance measures used to represent a computer system performance.
b) Elucidate the functioning of a Micro program sequencer. [5+5]

OR

12 a) Formulate a mapping procedure that provides eight consecutive micro instructions for fetch routine. The operation code has 7 bits and control memory has 4096 words.
b) Explain common bus system. [5+5]

13 a) Explain the register organization in 8086.
b) Discuss about the data bus and address bus in 8086 processor? [5+5]

OR

14 a) Explain the pin configuration details of 8086.
b) Explain the assembler directives with examples. [5+5]

15 a) Is 'c' an assembly language? Justify your answer.
b) With an assembly language program explain stack organization in 8086. [4+6]

OR

16 How to pass parameters to procedures in 8086? Explain in detail with an ALP. [10]

17 Explain Booths multiplication algorithm with example. [10]

OR

18 Compare interrupt driven data transfer scheme with DMA. Using block diagram explain interrupt driven transfer scheme. [10]

19 a) With the help of a neat diagram explain the match logic for one word of associative memory.

b) What are the various forms available for establishing an interconnection network in a multi processor system? [5+5]

OR

20 a) Distinguish between the virtual memory and cache memory. Write the merits and demerits of virtual memory.

b) Give a neat sketch that illustrates the components in a typical memory hierarchy. [5+5]