R17 Regulation *Subject code:* 1P4BA

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A' Grade)

B.Tech II Year II Semester Supplementary Examinations, July 2021

SWITCHING THEORY AND LOGIC DESIGN

(Electrical and Electronics Engineering)

Maximum Marks: 70 Date:18.07.2021 Duration: 3 hours

Note: **1.This question paper contains two parts A and B.**
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit which carries 10M.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks **(10x2M=20 Marks)**

1 What are the different illegal states of BCD and XS-3?
2 What are Universal logic gates?
3 Find the 2's complement of
i).11101010 ii) 01111110
4 Write down the truth table of Half-adder?
5 What is the difference between combinational and sequential circuits?
6 Draw the truth table of T-Flip-flip.
7 Define Shift register.
8 What is the difference between RAM and ROM?
9 What do you mean by Mealy model?
10 Define merger graph of n-state machine M.

Part-B

Answer All the following questions. **(10MX 5=50Marks)**

11 A. Derive the Hamming code for the sequence (1010) (5M)
B. Write the BCD code for $(543)_{10}$ and $(82.44)_{10}$ (5M)

OR

12 Simplify the following Boolean expressions using the Boolean theorems. (10M)
(i) (A+B+C) (B'+C) + (A+D) (A'+C) (ii) (A+B) (A+B') (A'+B)

13 Obtain the simplified expression in POS (product of sums) of
$F(w,x,y,z)=\pi(2,4,6,12,13,15)$ using K-maps. (10M)

OR

14 a) Design the Full-Adder. (5M)
b) Define a multiplexer? Draw 2:1 multiplexer for the function $f(x,y,z)=\sum(0,1,3,6,7)$ (5M)

15 a) Explain JK Flip-flop with neat sketches and excitation table. (5M)
b) Explain Race around condition and how it is eliminated. (5M)

OR

16 a) Convert SR flip flop to JK flip flop. (5M)
b) What is the difference between D-latch and D-flip flop. (5M)

17 a) Explain about serial in parallel out shift register with a neat diagram. (5M)
b) Design a synchronous counter with T-flip flops that goes through the binary repeated sequence 0,1,3,7,6,4,0,1….. (5M)

OR

18 Design 4 bit Ring counter. (10M)

19 a) What are the Moore and Mealy machines? Compare them. (5M)
b) Explain the procedure for state minimization using the partition technique. (5M)

OR

20 a) Write the steps in analyzing of sequential circuit. (5M)
b) write the procedure for synthesis of finite state machines. (5M)