R18 Regulation

*Subject code:*2P3DB

TKR COLLEGE OF ENGINEERING AND TECHNOLOGY

(Autonomous, Accredited by NAAC with 'A' Grade)

B.Tech III Semester Regular/Supplementary Examinations, February 2021

DIGITAL LOGIC DESIGN
(Electronics and Communication Engineering)

Maximum Marks: 70

Date: 19.02.2021 **Duration: 3 hours**

Note: **1.This question paper contains two parts A and B.**
2. Part A is compulsory which carries 20 marks. Answer all questions in Part A.
3. Part B consists of 5 Units. Answer any one full question from each unit which carries 10M.
4. Each question carries 10 marks and may have a, b, c, d as sub questions.

Part-A

All the following questions carry equal marks **(10x2M=20 Marks)**

1 What is Gray code?
2 Distinguish between the canonical and standard forms by giving an example
3 Draw the logic circuit of half Adder & mention the truth table
4 What is an important of priority Encoder
5 What are the basic difference between combinational logic circuit andsequential circuit
6 Differentiate between latch and flip flop
7 Define a universal shift register
8 Compare asynchronous and synchronous counters.
9 Define finite state machine
10 What Is Moore and Mealy machine compare them

Part-B

Answer All the following questions. **(10MX 5=50Marks)**

11 A. Convert the gray number 101101into decimal, hex, octal 5M
B. Perform the subtraction in BCD using 9's complement method for 592.6-887.9 5M

OR

12 Design a circuit to convert Excess-3 code to BCD code using discrete Logic gates . 10M

13 A.Simplify the following Boolean functions using a four vriable K-Map method 5M
$F(A,B,C,D) = \sum m(0,2,4,5,6,7,10,11,15)$

B.Draw the Multiple level NOR gate circuit for the Following expression w(x+y+z)+xyz 5M

OR

14 A. Construct a 16x1 multiplexer with two 8x1 and one 2x1 multiplexer use block diagram 5M
B. Draw the logic diagram of a 2 to 4 line decoder using NOR gates only include enable input 5M

15 A. Explain about a NOR Latch in detail with a neat diagram. 5M
B. What are the difference between the Sequential circuit and combinational circuit? 5M

16 A. Draw the SR Latch logic diagram with NAND gates. Explain using truth table 5M

OR

B. Briefly Explain the positive edge triggered D-Flip-flop. 5M

17 A. Convert D flip-flop into T flip-flop . 5M

B. Explain about Ring counter With neat sketches. 5M

OR

18 A. Design 4-bit synchronous up-counter with T-flip flop. Explain its working. 5M

B. How to realize the switching functions using PLDs. Explain. 5M

19 A. Demine the Condition under which two equivalent machines are isomorphic. 5M

B. Compare Moore and Melay machines. 5M

OR

20 Draw the logic diagram of Mealy and Moore models and also explain their operation with examples (10M)